A 5.8 GHz Fully-Integrated Power Amplifier for 802.11a WLAN System

G. C. Lin and Z. M. Lin

***Abstract*-In this paper, a 5.8 GHz fully-integrated power amplifier is designed and implemented in a 0.18-μm radio frequency CMOS process. The power amplifier is formed by a cascaded class-D pre-amplifier and a class-E amplifier to drive the output power stage. The designed PA delivered an output power of 13.86 dBm with a power-added efficiency (PAE) of 20% and a power gain of 26.66 dB.**

I. INTRODUCTION

The growing demands for high throughput in wireless local area networks (WLANs) has generated increasing interest in the IEEE 802.11a [l] standards. This protocol provides data rates up to 54Mb/s using a 20-MHz channel bandwidth in the 5-GHz unlicensed national information infrastructure (UNII) hand.

Wireless transmitters often utilize power amplifiers (PA_S) as the final amplification stage. Together with the high gain provided, the nonlinear PA_S also cause distortions to the input signal both in-hand and out-of-hand, which have serious impact on the communication quality. Therefore, accurate PA modeling is needed to help troubleshoot the impairments and optimize the trade-off between the efficiency and nonlinearity [2]. A tradeoff exists between efficiency and linearity in conventional switching PAs and conducting PAs. Switching PAs, such as class-D, -E, and -F are very efficient, but highly non-linear [3]. On the other hand, conducting PAs, such as class-A, -B, and -C are highly linear but are very inefficient [4].

This work investigates the feasibility of designing a class-E PA with a high gain pre-amplifier to achieve high efficient and high PAE for WLAN system. Section III presents the designed PA and points out the main design problems. Section IV presents the simulation results of the proposed PA and final conclusions are given in section V.

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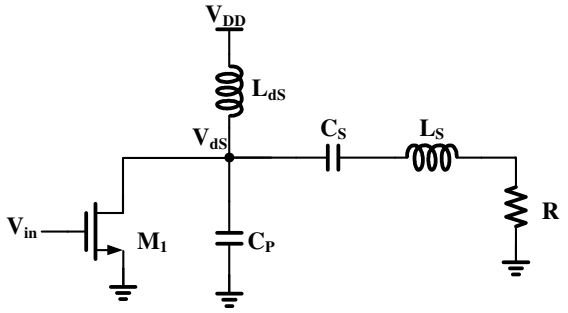

Fig. 1. A basic class-E stage.

II. CLASS-E OPERATION

Fig. 1 shows a class-E PA stage. The active device operates as a switch. The input signal Vin toggles the switch periodically with approximately 50% duty cycle. When the switch M_1 is on, a linearly increasing current is built up through the inductor L_{dS}. At the moment M_1 is turned off, this current is steered into the capacitor C_P, causing the voltage across the switch V_{ds} to rise. The tuned network is designed such that in steady state, V_{dS} returns to zero with a zero slope, immediately before M_1 is turned on. C_S and L_S operates as the band-pass filter and selectively passes the fundamental component of V_{dS} to the load, creating a sinusoidal output that is synchronized in phase and frequency with the input. In addition, the switch voltage and the switch current are never simultaneously nonzero. Since the instantaneous power dissipation of the switch is the product of these two quantities, the switch is ideally lossless, and all the power from the dc supply is delivered to the radio-frequency output.

III. CIRCUIT DESIGN

A schematic of the designed PA is shown in Fig. 2. The output stage of the power amplifier is a class-E amplifier, and the driver stage is a pre-amplifier that is composed of a cascaded class-D amplifier.

A class-E stage would require a square wave driving signal that the class-D [5] chains are used in order to meet the demand. In addition, a class-D amplifier has the highest gain when the biases of the input and output are set to the mid-point between V_{DD} and the ground.

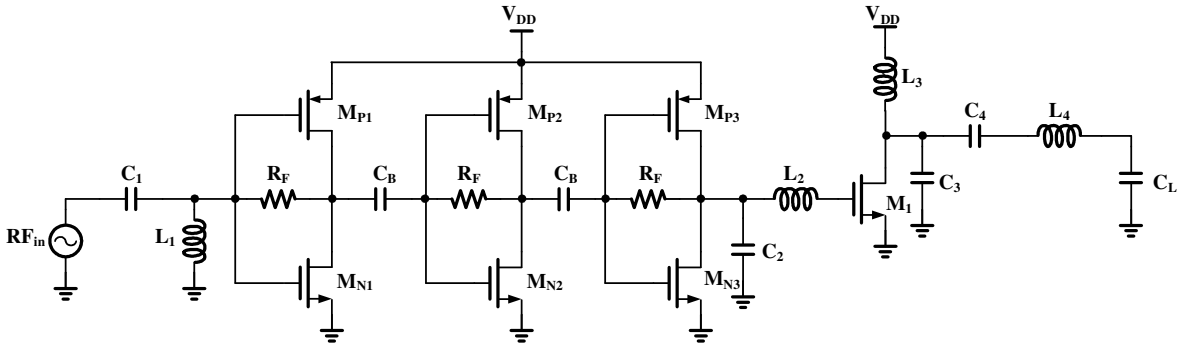

Fig. 2. Schematic of the designed PA

The input and the output of each class-D amplifier are connected through a feedback resistor R_F in order to equalize the bias of the output to the bias of the input. To separate the bias of each class-D amplifier, class-D amplifiers are cascaded through dc blocking capacitors C_B. By doing this, the gain degradation of each amplifier is prevented. As the output bias of the last class-D amplifier is used for the input bias of the power stage, no additional gate bias of the power transistors is needed. The transistor of each class-D amplifier is two times larger than that of the previous class-D amplifier and the size of the first one is set very small. Thus the gain of the power amplifier could be elevated.

The output stage used a traditional class-E amplifier. The size of M_1 is designed as large as possible in order to obtain higher output power.

IV. Simulation Results

The performance of the PA was simulated using Advance Design System (ADS) software with 1.8V supply voltage in TMSC CMOS 0.18-µm technology. Fig. 3 shows the chip layout photograph of the PA.

A small-signal gain of more than 27.5 dB is simulated at 5.8 GHz, as shown in Fig. 4. The input reflection coefficient S11 and output reflection coefficient S22 are better than -14 dB over the frequency band as shown in Fig. 5.

Fig. 6 shows the output power and PAE performance with a single-tone input signal. A 15.7 dBm saturated output power is achieved with a maximum PAE of 25.1%. As depicted in Fig. 7, the power gain and output power of P_{1dB} are 26.66 dB and 13.86 dBm, respectively. 20% PAE is achieved with that output power of P_{1dB} as shown in Fig. 8.

Fig. 9 exhibits the total current in accordance with an output power and the power amplifier uses a low quiescent current of Class AB mode in this work. The total current of 67 mA is achieved with the output power of P_{1dB}. As shown in Fig. 10, the simulated third-order IMD which is frequency- dependent distortion is less than -42 dBc for the frequency 5.8 GHz. Table I shows the summary of the performances compared with the reported works.

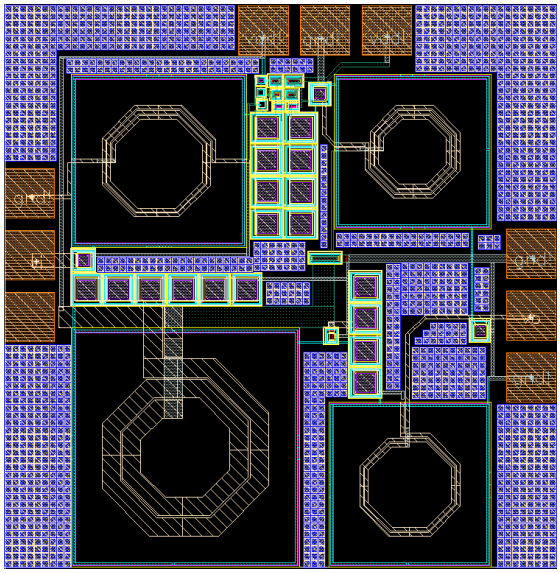

Fig. 3. Layout of the PA.

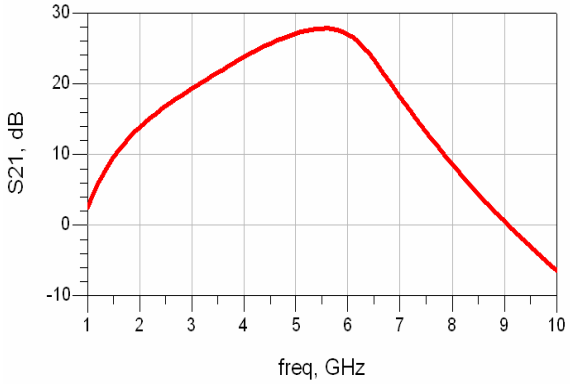

Fig. 4. Small-signal gain of the class-E power amplifier at V_{DD}=1.8V.

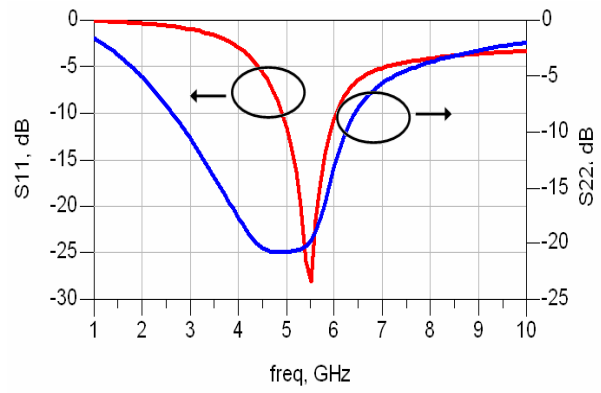

Fig. 5. Input return loss and output return loss of the class-E power amplifier at V_{DD}=1.8V.

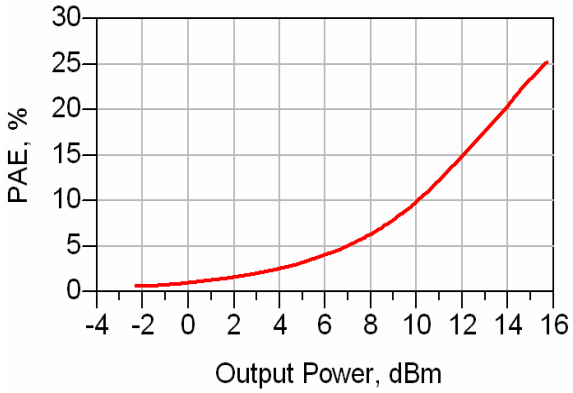

Fig. 8 PAE versus output power.

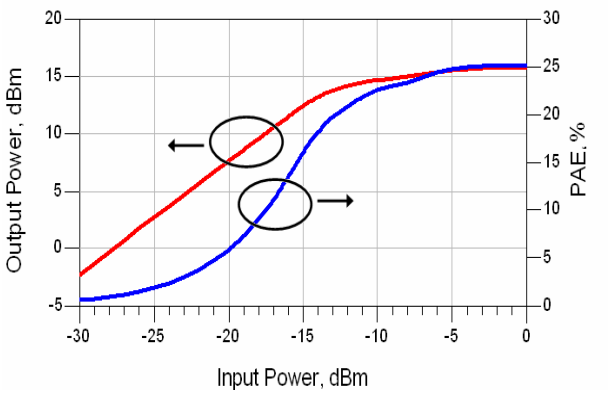

Fig. 6. Output power and PAE versus input power.

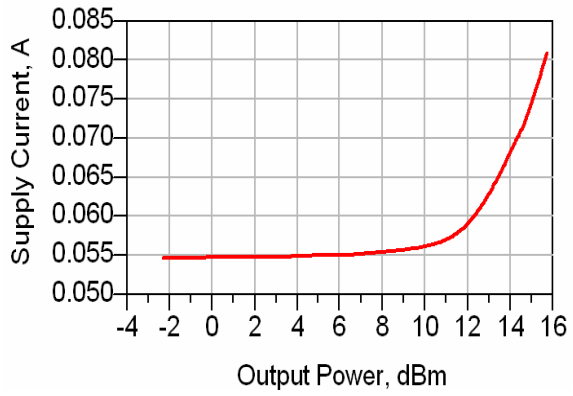

Fig. 9. Supply current versus output power.

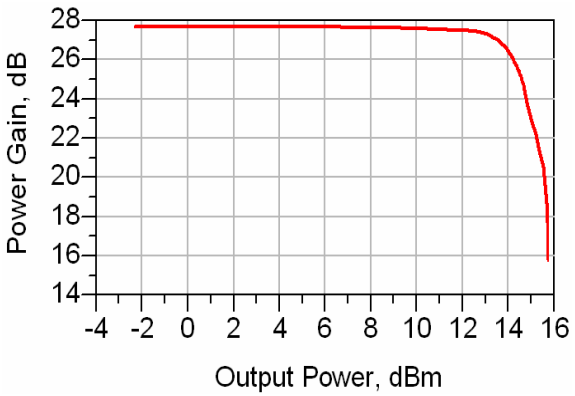

Fig. 7. Power gain versus output power.

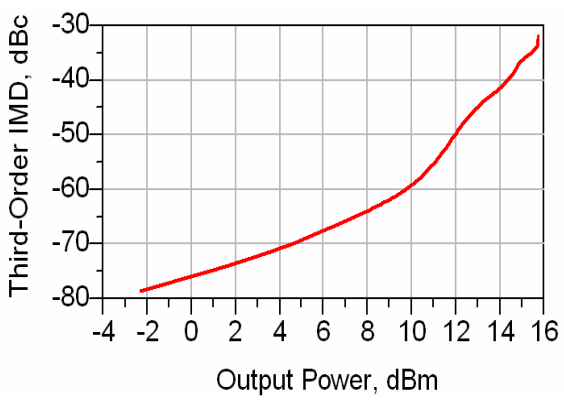

Fig. 10. Third-order IMD corresponding to output power.

TABLE I COMPARISON OF PA PERFORMANCE

	[6]	[7]	[8]	**This work**
Process	0.18μm	0.18μm	0.18μm	**0.18μm**
Frequency(GHz)	5	1.95	5.85	**5.8**
Supply Voltage(V)	3.3	1.8	3.3	**1.8**
Power Gain(dB)	25.5	15	18.5	**26.66**
$P_{out\text{-}1dB}$(dBm)	20.8	20	25	**13.86**
PAE(%)	26.7	42.2	20	**20**
P_{diss}(total)(mW)	528	207	339.9	**120.6**
Size(mm^2)	1.1×2.2	-	1.4×0.8	**0.9×0.9**

V. CONCLUSION

A 5.8 GHz class-E CMOS PA fabricated in a TSMC 0.18um standard CMOS process with a cascaded class-D pre-amplifier for IEEE 802.11a WLAN application is presented. High gain and low quiescent current are achieved by using the cascaded class-D amplifier and the application of the proposed composition. A total power dissipation of 120.6 mW is consumed for an output power of 15.7 dBm with a maximum PAE of 25.1%. The power amplifier exhibits 26.66 dB power gain, 13.86 dBm P_{1dB}, and 20% PAE. The third-order IMD is less than -42 dBc with the output P_{ldB} for the frequency of 5.8 GHz.

ACKNOWLEDGEMENT

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